REMARKS

Claims 1, 2, 7, 8-10, 12 and 15 stand rejected under 35 USC §102(e) as being anticipated by Miller, U.S. patent 6,603,323. Claims 1-15 stand rejected under 35 USC §102(e) as being anticipated by Rutten, U.S. patent 6,747,469. Claims 1-15 stand rejected under 35 USC §102(e) as being anticipated by Wiscombe et al., U.S. patent 5,014,002.

Claims 1, 3, 5, 7, 9, and 15 have been amended to more clearly state the invention. Claims 2, 6, 10, and 11 have been cancelled. Reconsideration and allowance of each of the pending claims 1, 3-5, 7-9, and 12-15, as amended, is respectfully requested.

Miller, U.S. patent 6,603,323 discloses an interconnect structure that employs a closed-grid bus to link an integrated circuit tester channel to an array of input/output (I/O) pads on a semiconductor wafer so that the tester channel can concurrently communicate with all of the I/O pads. The interconnect structure includes a circuit board implementing an array of bus nodes, each corresponding to a separate one of the I/O pads. The circuit board includes at least two layers. Traces mounted on a first layer form a set of first daisy-chain buses, each linking all bus nodes of a separate row of the bus node array. Traces mounted on a second circuit board layer form a set of second daisy-chain buses, each linking all bus nodes of a separate column of the bus node array. Vias and other circuit board interconnect ends of the first and second daisy-chain buses so that they form the closed-grid bus. Each bus node is connected though a separate isolation resistor to a separate contact pad mounted on a

surface of the circuit board. A set of spring contacts or probes link each contact pad to a separate one of the I/O pads on the wafer.

Rutten, U.S. patent 6,747,469 discloses a test system that is configured to include a preconditioning integrated circuit that is coupled between automatic test equipment (ATE) and a device-under-test (DUT). The preconditioning integrated circuit is configured to precondition signals that are communicated to and from the device-under-test, and particularly, to precondition high-frequency signals so as to avoid the adverse affects caused by long lead lines between the automated test equipment and the device-under-test. The preconditioning integrated circuit is designed to provide direct contact with the device-under-test, thereby providing very short lead lines to the device-under-test. High-frequency signals that are communicated to the device-under-test are generated, or reformed, at the preconditioning integrated circuit, based on control signals, or other test signals, from the automated test equipment. High-frequency, or time-critical, signals that are received from the device-under-test are processed and/or reformed by the preconditioning integrated circuit, for subsequent transmission to the automated test equipment.

Wiscombe et al., U.S. patent 5,014,002 discloses that relays and toggle switches for programming the electrical interconnections between automated test equipment and the pins of a DUT are replaced with manually programmable jumpers connected between various jumper terminals mounted on a jumper programmable interface board. The jumper terminals are located on the interface board in close proximity to the pins of a DUT to minimize interference and crosstalk. Pulldown and

pullup resistors as well as bypass capacitors are optionally incorporated into the jumpers. The jumper terminals provide easy access to pin electronics (PE) test signals and to various power and ground plane in a multilayer interface board so that the test conditions for each pin can be manually programmed by selection of jumper connections.

Independent claims 1 and 9 respectively recite a method and apparatus for implementing multiple signals probing of a printed circuit board. Applicants respectfully submit that as amended, each of the independent claims 1 and 9 is patentable over the references of record.

The method and apparatus for implementing multiple signals probing of the present invention as recited by each of the independent claims 1 and 9, as presented, enables better access to an area of interest on the printed circuit board for probing and connecting to signals than prior art arrangements, such as disclosed by Miller et al., Rutten, and Wiscombe et al. The probe structure of the present invention is integrated directly onto the printed circuit board, utilizing the manufacturing processes already used to build the printed circuit board, and essentially no additional cost is incurred during the manufacture of the printed circuit board. The design of the probe structure of the present invention takes minimal effort during the computer aided design (CAD) layout phase of the PCB design.

As amended, independent claim 1 recites the steps of providing a pattern of vias in the printed circuit board including multiple predefined vias, each said predefined via being connected to a respective signal to be monitored; forming a probe

structure on an outside surface of the printed circuit board including a pattern of a plurality of spaced apart electrically conductive stubs, each stub including an elongated portion extending from at least one pad, and said pattern including one of said plurality of stubs adjacent each said predefined via connected to said respective signal to be monitored; electrically connecting a resistor between one said predefined via connected to one said respective signal to be monitored and said adjacent stub; and defining a path to a predefined probe location on the printed circuit board for monitoring said signal from said resistor using said probe structure by placing zero-ohm shorts between selected ones of said pads of said plurality of stubs of said probe structure.

As amended, independent claim 9 recites a pattern of vias in the printed circuit board including multiple predefined vias, each said predefined via being connected to a respective signal to be monitored; a probe structure formed on an outside surface of the printed circuit board; said probe structure including an electrically conductive material forming a pattern of a plurality of spaced apart stubs defining said probe structure on said outside surface of the printed circuit board, each said stub including an elongated portion extending from at least one pad; said pattern including one of said plurality of stubs adjacent each said predefined via connected to said respective signal to be monitored; a resistor electrically connected between one said predefined via connected to one said respective signal to be monitored and said adjacent stub; and a path defined to a predefined probe location for monitoring said signal from said resistor using said probe structure; said path being formed by electrically shorting between said pads of selected ones of said plurality of spaced apart stubs.

As recited in each of the independent claims 1 and 9, as amended, the probe structure is formed on an outside surface of the printed circuit board; said probe structure including an electrically conductive material forming a pattern of a plurality of spaced apart stubs defining said probe structure on said outside surface of the printed circuit board, each said stub including an elongated portion extending from at least one pad; said pattern including one of said plurality of stubs adjacent each said predefined via connected to said respective signal to be monitored.

Applicants respectfully submit that the references of record do not disclose, nor suggest the probe structure as taught by the present invention and recited in each of the independent claims 1 and 9, as amended. Applicants respectfully submit that each of the independent claims 1 and 9, as amended, is patentable over all the references of record including Miller et al., Rutten, and Wiscombe et al.

As recited in each of the independent claims 1 and 9, as amended, a resistor electrically connected between one said predefined via connected to one said respective signal to be monitored and said adjacent stub. Applicants respectfully submit that the references of record including Miller et al., Rutten, and Wiscombe et al. do not disclose, nor suggest the resistor used with the probe structure as taught by the present invention and claimed in each of the independent claims 1 and 9, as amended. Thus, each of the independent claims 1 and 9, as amended, is not suggested by and is patentable over Miller et al., Rutten, and Wiscombe et al.

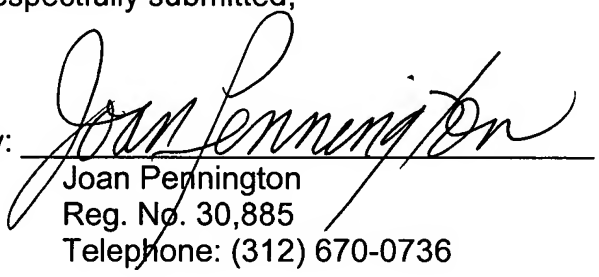
Each of the dependent claims 23-5, 7-9, and 12-15 further define the subject matter of patentable claims 1 and 9, and each is patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1, 3-5, 7-9, and 12-15, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

By: 

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